Exam 2
EE3410 Electronics 2
Spring 2025

Overview: This exam asks you to analyze an operational amplifier using both hand and computer calculations. The analysis will investigate the figures of merit of the amplifier and characterize its performance. ALL ANALYSIS SHOULD BE DONE WITH C9=15pF UNLESS OTHERWISE NOTED. C9 is the compensation capacitor. It is used to ensure amplifier stability.

Circuit: The circuit to be analyzed is provided in a separate post. The filename is 'Exam_2_OPAMP_LTSPICE. This file is compatible with the LTSPICE program. You will need to modify the file slightly as you go through the analysis. The file as provided is configured as a non-inverting amplifier as shown in the diagram below. Components R15 and R16 are components external to the operational amplifier circuit that are used to set the gain. The file as provided has these components selected to provide an inverting gain of 10.

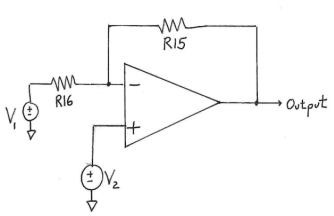

Figure 1: Circuit Connection

Problem 1: Circuit Description

Describe the different stages and subcircuits of this amplifier in a few paragraphs.

Include a description of each of the amplifier stages. For each stage list the transistors and passive components used in that stage. List the topology of that stage (e.g. common emitter, differential amplifier, cascade amplifier, emitter follower, SOURCE FOLLOWER, ect.) Describe the function of the stage. Describe the bias circuitry separately. If a current source is used to bias a stage identify the type of current source (e.g. Widlar, Wilson)

If you do not know the function of a component, make a note in your description.

Differential Amp

The first stage of the op-amp is the differential pair of Q1 and Q2. This differential pair is being constant current biased by the current source of Q3. The operating points of the collector are chosen by R1 and R2 as the current should be relatively the same in both branches. R3 and R4 provide a way to balance the offset produced by Q4 and the output of this stage drawing different amounts of current. The diode D1 is being used as temperature compensation, the voltage across the diode decreases with temperature which compensate for the other temperature differences in this stage (I am not 100% sure on this). The output is taken one sided on the collector of Q2 and fed to the next stage. The inputs are applied at the bases of Q1 and Q2.

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Cascode Amp

The next stage is a cascode amplifier configuration consisting of Q5 and Q6. This is the main gain stage of the differential amplifier. Q5 is a common emitter amplifier as the output is being taken on the collector of this transistor. It has a resistive load being R12. The common emitter is being used for its high gain properties. The common base circuit is being biased by R13 and 14. There is also a bypass capacitor in parallel to R13 so more gain can be produced whilst keeping the circuit stable. The output of the common emitter goes to the input of the common base. A common base is used to get more gain, a higher output resistance, and a higher frequency response.

JFET

Buffer with a gain of 1, high input impedance, low output impedance

The JFET is used here as a voltage buffer. The cascode amplifier produces high gain but also high output resistance, but the JFET has a higher input impedance, so it receives most of the signal. Without this stage most of the signal would be lost in the output resistance of the cascode amplifier. The JFET also has low output resistance, so the final stage can receive most of the signal.

Class AB Power Output

The class AB power output stage is likely chosen for its high efficiency of 50-70%, its low output impedance, and very low crossover distortion. The high efficiency ensures minimal power is lost in the output stage, the low output impedance makes sure that whatever the load of the circuit is gets most of the signal, and the low crossover distortion is from both transistors being on for more than half of the cycle.

Bias Circuitry

The differential stage, cascode stage, and power output stage are being constant current biased by Q3, Q7, and Q9 respectively. It's pretty cool how this works, more on that later. Resistors R6 and R7 are setting the "reference current" for these circuits which is really just setting the base voltage. Resistors R5, R8, and R9 control how much current goes through Q3, Q7, and Q9 respectively. The diode D4 is also used for temperature compensation similar to the diode in the differential input stage.

Problem 2: Model Verification

The models for each of the transistors are given as SPICE directives at the top of the schematic. You can find copies of the datasheets online, you will need these to compare the SPICE models to the manufacturer's specification.

Run an operating point analysis of the circuit. Identify the currents in each of the transistors. Populate the table below with these values. Also populate the remaining entries from the data sheet. **In the s** there is no Q8.

Notice that transistor J1 is a Junction Field Effect Transistor (JFET). You can read about this type of device in your text. Like a MOSFET the JFET is a field effect device. The construction of a JFET is such

that it is on with 0V gate to source voltage and requires a negative gate to source voltage to turn off. For J1 indicate if the analysis is consistent with the datasheet.

Table 1: Transistor Operating Points

Transistor	Spice Operating Point Analysis			Calculated β	Datasheet β	Comments
	Ic	Ib	Ie			
Q1	8.64uA	3.35nA	8.64uA	2580.10	900 min	Consistent. No max listed, but this is consistent with the Ic of 10uA on the datasheet
Q2	8.71uA	3.38nA	8.72uA	2580.34	900 min	Consistent. No max listed, but this is consistent with the Ic of 10uA on the datasheet
Q3	17.4uA	56nA	17.4uA	310.19	100-400 @ 100uA	Consistent. This value is in range. Does not explicitly say for smaller currents, but this is within range of this listing.
Q4	34.4uA	69nA	34.5uA	499.28	250-700 @ 100uA	Consistent, the collector current is not the same, but it is within this range.
Q5	45.6uA	107nA	45.8uA	427.10	250-700 @ 100uA	Consistent, the collector current is not the same, but it is within this range.
Q6	45.6uA	90.6nA	45.6uA	502.79	250-700 @ 100uA	Consistent, the collector current is not the same, but it is within this range.
Q7	45.6uA	148nA	45.7uA	308.23	100-400 @ 100uA	Consistent, this is within the range for 100uA, but it is not tested lower.
Q9	2mA	6.43uA	2.01mA	311.43	100-400 @ 100uA	Consistent if we look at the max an min for 100uA of current, but the current is a lot larger here. There is no measurement for 1mA of current, so it is hard to say if it is truly consistent.
Q10	131uA	1.13uA	132uA	115.72	min 35 @ 100uA	Consistent, but hard to say because there is no listed upper limit to what this value can be. It is listed that with 150mA, the max is 300, so with this range, 115.72 seems reasonable.

Q11	132uA	450nA	132uA	292.48	Min 35 @ 100uA	Consistent. Similar issue where 35 is the minimum for a similar current, but no maximum is listed. A maximum of 300 is listed for a current of 150mA, and this value is within this range, so I will say it is consistent.
Q12	1.49pA	1.44pA	48fA	-1.03	100-400 @ 100uA	Not consistent. The beta is negative and the base and collector currents are larger than the emitter. The transistor appears to be off here
Q13	875fA	836fA	38.9fA	-1.05	250-700 @ 100uA	Not consistent. This could be because of the transistor being off. The emitter current again is smaller than the base and collector currents.
Q14	There	Is	No	Q	1	4

Transistor	I_D	I_S	V_{GS}	Comments
J1	2mA	2mA	-2.3534	Consistent. Range of -2.0->(-6.0)V. This is within range and the JFET is on.

Problem 3: Current Source Analysis

Perform a hand calculation for each of the current sources in the circuit. (There are three, one associated with Q3, one with Q7 and one with Q9). Show your circuit diagrams and calculations. Enter the results in the table below. Determine the output resistance of each current source. (You can use LTSPICE to determine the output resistance). Enter the results in the table below. In the comment column indicate if your calculation agree with LTSPICE.

Provide a paragraph or two of discussion describing how the current sources work and how you did the analysis.

Table 2: Current Source Bias Points

Current Source	Output Current Hand calculation	Output Current LTSPICE	Output Resistance	Comments
Q3	17.92uA	17.363uA	498.01MOhms	Agree
Q7	47.06uA	45.636uA	185.19MOhms	Agree
Q9	2.067mA	2.003mA	4.08MOhms	Agree

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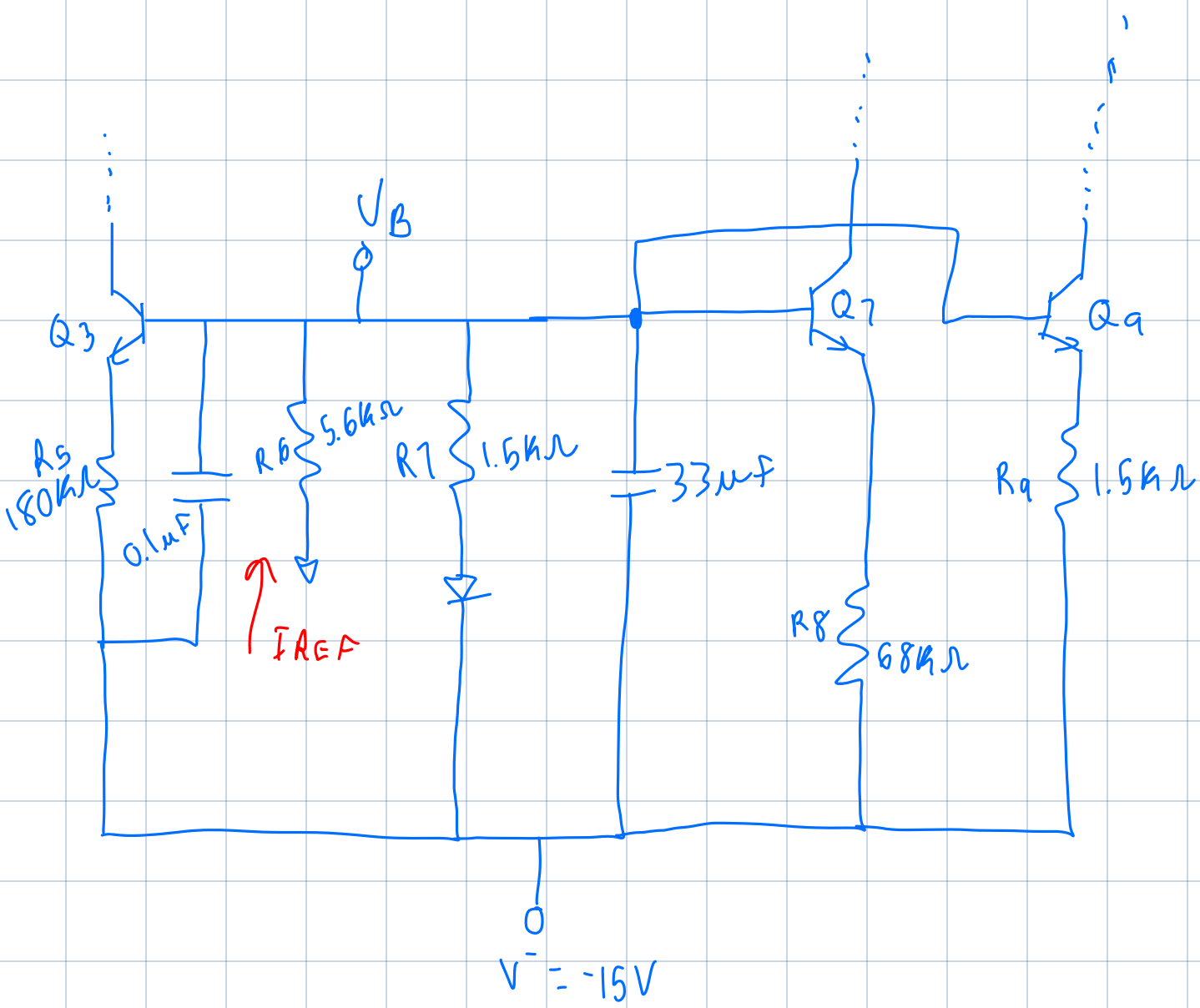
To calculate the bias currents in each current source I first recognized that the current that is driving these transistors is coming out of ground and going through R6. In my analysis I chose to ignore the base currents as the betas for these transistors are all over 300, I will of course go back and check my assumption. With this assumption, all the current going through R6 will also be going through R7. Using KCL I found the current going through these resisters and with the this current I found the shared base voltage. With the base voltage, I then used KVL and the equation for diode current on each transistor to find the collector current:

$$I_{CQX} = I_S e^{V_{BE(QX)}/V_T}$$

$$V_B - V_{BE} - I_{CQX} R_X = V^-$$

The X subscript indicates the resistor number and transistor number: Q3 with R5, Q7 with R8, and Q9 with R9. Plugging one equation into the other gives the collector current

To calculate the output resistance, I copied the current sources to in LTspice and connected them to the negative supply, the same as the original circuit. I then connected all the collectors together and connected a voltage source to them. I then ran a linear dc sweep and plotted the collector currents against the collector voltage. The inverse of the slope of this graph gave me the output resistance of each current source.



assume base current small, so

$I_{REF} \cong I_{R7}$

V^-

$0 - I_{REF} R_6 - I_{REF} R_7 - V_\gamma = -15$

$$15 = I_{REF}(R_6 + R_7) + V_\gamma$$

$$I_{REF} = \frac{V^- - V\gamma}{R_6 + R_7} \approx 2.01\,mA$$

$$V_B = 0 - I_{REF} R_6 = -11.256\,V$$

Q_3 — ignore base current

$$V_B - V_{BE} - I_C R_5 = -15$$

$$I_C = I_S e^{V_{BE}/V_T}$$

Wolfram:

$$V_{BE} = 0.519\,V$$

$$I_{CQ3} \approx \frac{V_B - V_{BE} - V^-}{R_5} = 17.92\,\mu A$$

Q_7

$$V_B - V_{BE} - I_C R_8 = -15$$

$$I_C = I_S e^{V_{BE}/V_T} \rightarrow V_{BE} = V_T \ln\left(\frac{I_C}{I_S}\right)$$

$$V_{BE} = 0.5442$$

$$I_{Q_7} = \frac{V_B - V_{BE} - V^-}{R_8} = 47.06\,\mu A$$

Q_9

$$V_{BE} = 0.643V$$

$$I_C = 2.067mA$$

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Problem 4: Gain

Perform an AC analysis and calculate the DC gain of each stage. List the gain and amplifier type for each stage in the table below. You will need to decide whether to do this analysis in an open loop configuration (R15 and R16 not present and the input tied directly to the base of the input transistor) or in a closed loop configuration using R15 and R16. However, the values you enter in the table below should be the open loop gain. Attempt to determine the 3dB point of each gain stage separately. **For all these calculations set the compensating capacitor C9 to 15pF.**

Table 3: Stage Gains

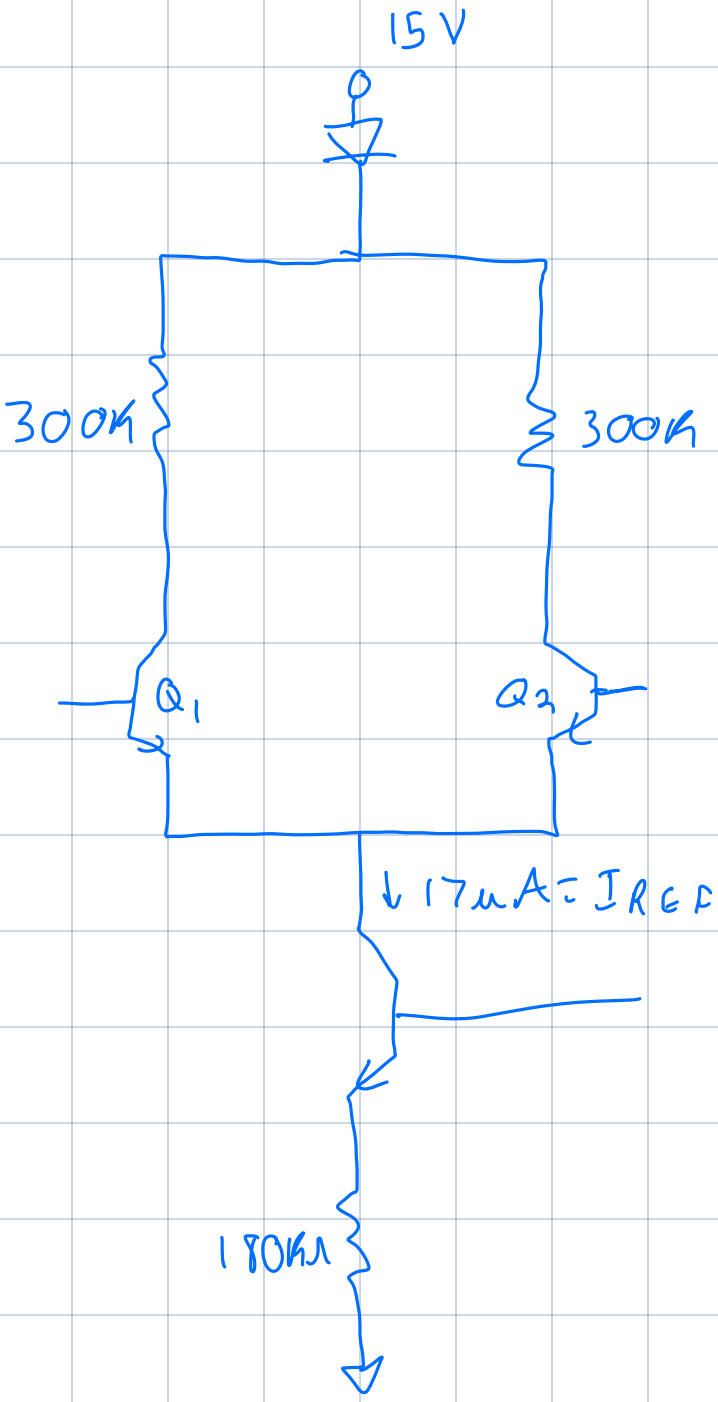
	Type of Amplifier	DC Gain (dB)	High Frequency 3dB point
Stage 1	One sided Differential	51.2	669.23mHz
Stage 2	Cascode (Common Emitter/Base	85	5Hz
Stage 3	Buffer	-2mdB	382kHz
Stage 4	Class AB output	-11mdB	Around the GHz range

Problem 5: Offset

Set your amplifier for a gain of 1000 by setting R15 to 100 kOhm and R16 to 100 Ohm. Ground the non-inverting input of your amplifier, and set the DC value of voltage source V1 to 0. In this configuration the offset (referred to the input) would be your output voltage divided by your closed loop gain. Record the value of this initial offset in the table below. Make sure you include the sign (+/-) of the offset.

Repeat this analysis with R15 set to 100 MOhm and R16 set to 100 kOhm. Record this value of offset into the table below. By how much did the offset differ? Enter this value into the last column of the table. Explain why the output changed even though our ideal gain was still 1000. Add a 100Kohm resistor between the non-inverting input and ground (call this R17) and measure the offset. You should find that the value now is near to the value measured with the 100K Ohm and 100 Ohm resistor you originally measured. Can you explain why? Attempt to explain why quantitatively. (Hint: Look at bias currents). Is the result consistent with the bias points analyzed earlier. If you were the selling this amplifier which value of offset would be more appropriate to include in the datasheet? Would you need to specify how the offset was measured?

The output changed because the current in the feedback stage is less. The offset changed when adding this new resistor because there is a similar amount of current in the feedback as there is in the non-inverting terminal, so the current offset in between the two inputs will be less. I tried to look at the bias currents but the base and collector currents looked the same, they were consistent with what I analyzed earlier.



$$V_C = V^+ - V_\gamma - \frac{I_{REF}}{2} R_C$$

$$= 15 - 0.7 - 8.5\mu A(300K) = 11.75V$$

max Cm when Q_1 or Q_2 sat

$$11.75 - V_{CE(SAT)} + V_{BE(on)} = V_{cm(max)}$$

$$11.75 + .7 - .2 = 12.25 \text{ V}$$

min when Q_3 sat

$$V_E = V^- + I_{REF} R_5 + V_{CEQ_3(SAT)}$$

$$= -15 + 17\mu A(180k) + 0.2 = -11.74$$

$$V_{BQ_1} = V_E + V_{BE(on)} = -11.74 + 0.7 = -11.04 \text{ V}$$

$$V_{CM(MIN)} = -11.04 \text{V}$$

$$V_{CM(MAX)} = 12.29 \text{V}$$

I think that the larger of the two offset values should be put on the datasheet because it is good to know the extrema of the parameters (it is also better to expect less and get a better offset to make the client happy). I think it would definitely be helpful to say the resistor values associated with measuring the offset, if someone wanted to verify their parts, they would be able to and if they find a problem they can contact the company and let them know.

Summarize your results in the table below:

Table 4: Offset Measurements

Configuration	R15 (Ohms)	R16 (Ohms)	R17 (Ohms)	Output (mV)	Offset referred to input (μV)	Difference from case 1 (μV)
1	100K	100	0	-231.95	-231.95	X
2	100M	100K	0	102.51	102.51	334.46
3	100M	100K	100K	-235.43	-235.43	0.52

Return the amplifier to configuration 1 in the table above. Now adjust R3 and R4 to get as small an offset as practical. (Try for less than 20 μV referred to the input, I got 3 μV in about 5 minutes of adjusting.) The sum of R3 and R4 should remain 50K Ohms. Enter your results in the table below:

Table 5: Offset Trim

R3	R4	Offset referred to input (μV)
23.525k	26.475k	.9285

Discussion: Look at the bias points of the amplifier in the original configuration. Look at base, collector and emitter currents and voltages. Where is the mismatch occurring that is causing the offset? You likely found that the magnitude of the offset in case 2 was less than case 1. This would seem to indicate that using larger value resistors in your circuit would reduce offset. Is this generally the case or does using larger value resistors generally cause more issues with offset? Discuss.

The discrepancy in current is from the base of Q4 and the output of the first stage drawing different amounts of current. Increasing the resistance does decrease the offset, but it can cause other problems as well. There is a small amount of current going into the two inputs and we want this ideally to be 0. The input current is defined by:

$$I_{in} = I_{feedback} - I_{inverting\ input}$$

We want the feedback and the inverting input currents to be the same or at least similar in magnitude. With larger resistors, the currents become smaller and closer in magnitude to I_in. If I_in is similar in magnitude, this indicates that there is a large difference between the two currents and this is will create a larger offset.

Problem 6: Common mode input range

Use the trim values for resistors R3 and R4 you found in Problem 6. Then configure your amplifier in an open loop configuration. Wire a common mode voltage to both inputs. Vary the input and try to determine the common mode input range of the amplifier. This is a bit tricky. Feel free to find another way to determine the common mode input range.

Work on next page

Problem 7: Stability

You will be analyzing the stability of the amplifier in various gain and compensation capacitor configurations as given in the table below. Wire your amplifier in an inverting amplifier configuration. You will need to pick reasonable values for resistors R15 and R16. Explain how you picked the resistor values. How did you pick resistors that were neither too small or too large?

I picked my resistors for a similar reason to the offset voltage question, large enough so the short circuit current would not be saturated, but small enough such that the magnitude of the feedback current and the input current would be larger than the current going into the input.

Provide a plot of the step response for several of the configurations. Use an amplitude of 5mV for your step. Use a rise and fall time of 50nS, and a pulse width of 150µS. Pick a representative set of plots to include in your exam.

Does there appear to be a relationship between closed loop gain and stability? If so, are the higher or lower gain configurations more stable?

It seems in general the higher gains are more stable until larger capacitors are added and they become very unstable and oscillate a lot (unless this is an LTspice bug).

Also calculate the maximum overshoot and settling time of the step response for each of the configurations. Record in the table.

Do an AC response of each of the configurations and record the gain bandwidth product in the table. Include one or two representative plots of the AC response in your submittal.

If you were going to include the compensation capacitor as part of your design (rather than have the user provide it) what would be a good all around value? Explain your reasoning. (Engineering is about tradeoffs, what tradeoffs are you making by picking a compensating capacitor rather than having the user pick it based upon their application). Your recommended value of compensating capacitor may not be any of the ones listed in the table. Play around and see what you can learn about compensation.

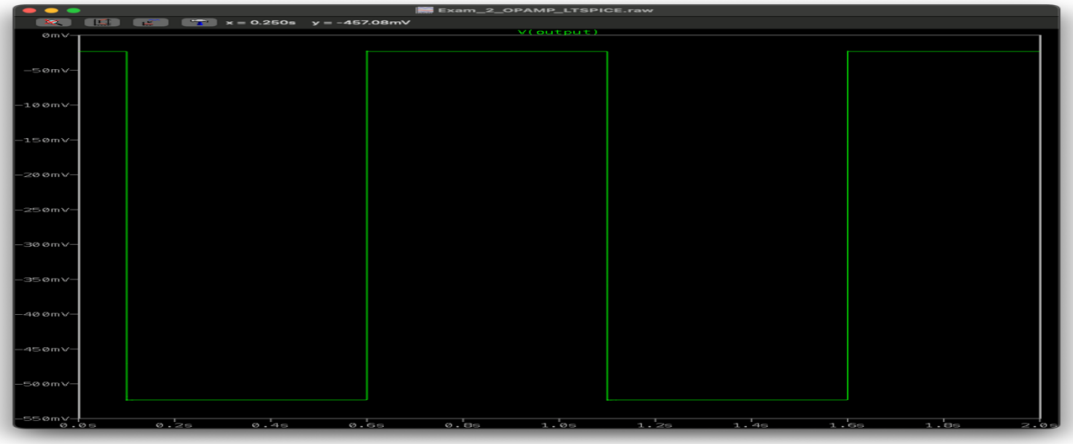
If I were to choose a capacitor value it would probably be around 15-20pF because there is a good trade off between settle time, overshoot, and gain-bandwidth product. Also, all configurations were becoming

unstable after a capacitor value of 20pF. I would choose 20pF as the bandwidth is not as relevant as the other figures of merit for a DC amplifier.

This section of the lab is tedious but not difficult. It is worth it to see the practical effects of compensation.

Table 5: Compensation

Configuration	Closed Loop Gain	R15	R16	Compensation Capacitor (pf)	Gain Bandwidth Product	Overshoot (%)	Settling time (ms)	Comments (Is the configuration stable?)
1	1	100k	100k	5	8.5MHz	30.8	12.8	No
2	100	100k	1k	5	5.7MHz	0.139	19.37	Yes
3	1	100k	100k	10	3.58MHz	21.25	6.9	NO
4	100	100k	1k	10	3.98MHz	0.143	14.19	Yes
5	1	100k	100k	15	653kHz	16.76	4.2	No
6	100	100k	1k	15	2MHz	0.0725	13.49	Yes
7	1	100k	100k	20	514kHz	9.36	3.5	No
8	100	100k	1k	20	2.2MHz	0.141	12.00	Yes
9	1	100k	100k	30	450kHz	9.74	2.25	No
10	100	100k	1k	30	800kHz	0.147	10.8	NO NO NO
11	1	100k	100k	50	407kHz	3.31	1.36	NO!!!
12	100	100k	1k	50	580kHz	0.23	9.36	NOPE



Iteration 2

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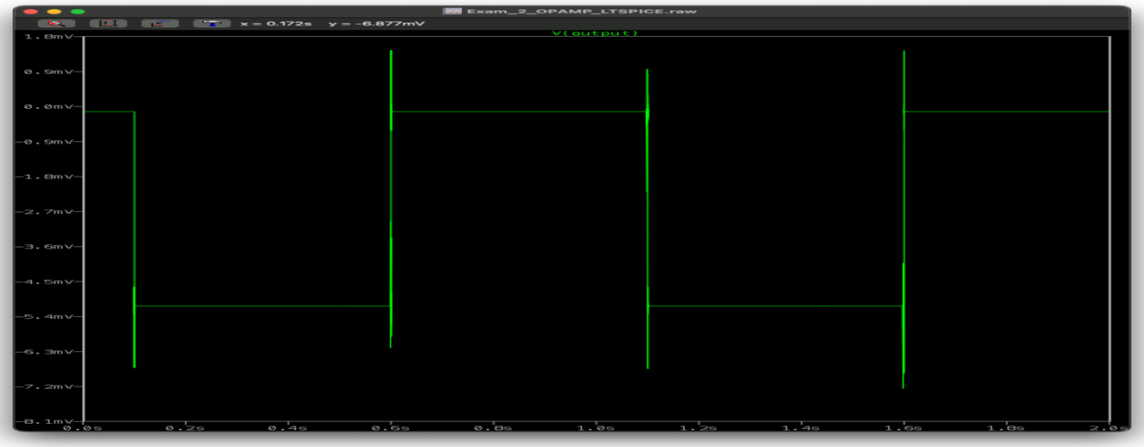
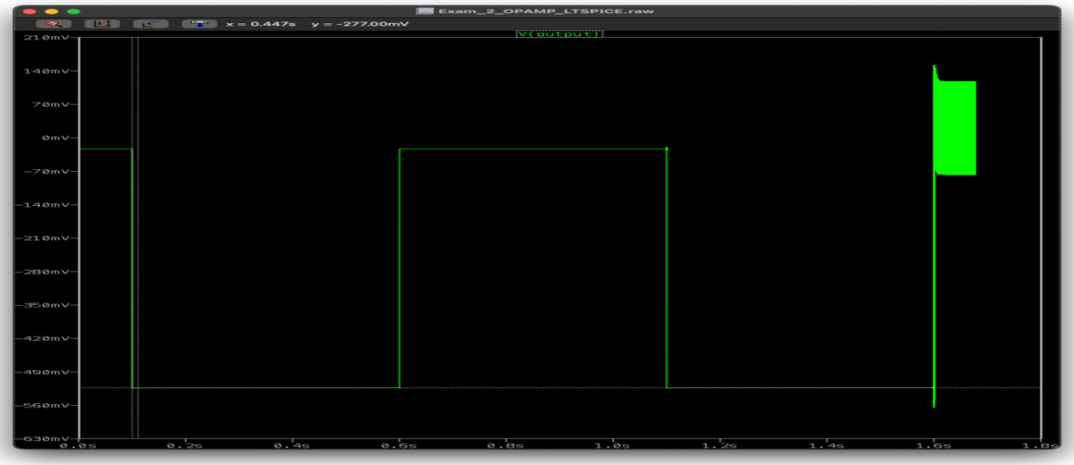
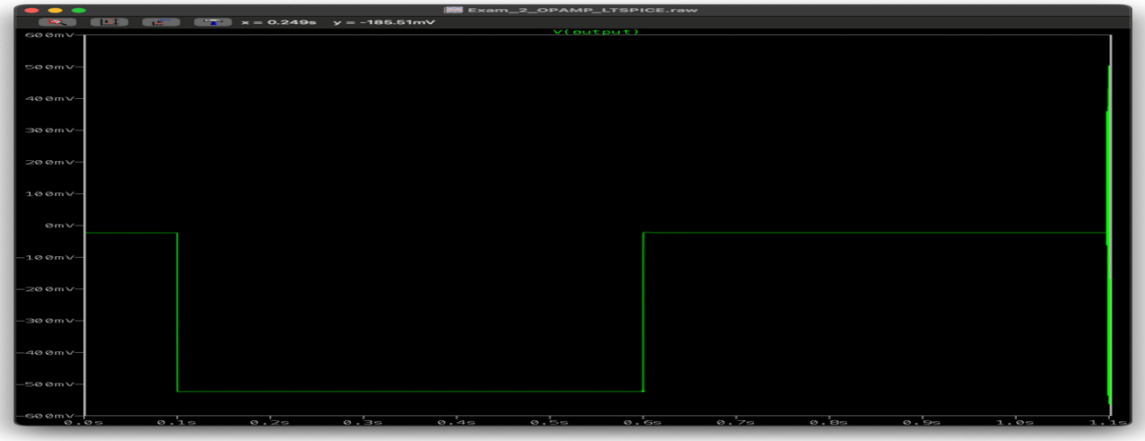


Iteration 1



Iteration 10



Iteration 12

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Problem 8: Large Signal Response and Slew rate

Configure your amplifier with a closed loop gain of 1 and input a pulse that starts at -10V and goes to 10V and then to -10V with a rise time of 50 nS, a 150 µS pulse width, and a 50nS fall time. You may want to delay the start of the pulse several microseconds to get a good plot of the rising edge.

Plot the step response of each of the configurations below and include in your exam submittal. Enter your summary data in the table below.

What tradeoffs are made by going to a larger compensation capacitor?

Do you see any unexplained behavior in your plot?

Using a large compensation capacitor causes a slower slew rate, but better stability. I saw a lot of oscillation using the 30pF capacitor after a few cycles showing the instability (or an LTspice bug).

Table 6: Large Signal Response

Configuration	Closed Loop Gain	Compensation Capacitor (pf)	Slew Rate (V/µS)	Comments (Is the configuration stable?)
1	1	5	1.727	Stable, only small transient
2	1	10	.865	Stable, Very small transient,
3	1	20	.434	stable, very small transient
4	1	30	.283	Stable minimal transient

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Problem 9: Output Swing

Pick a reasonably stable configuration from Table 6. Now add several values of load resistors from 100K ohms down to 100 ohms and repeat the step response analysis of table 6. (Connect the load resistor from the output to ground). What is the range of output voltage swings? Is the swing reduced from the 100K value even before the current limit is reached? (Another way of asking this is if the output swing depends upon the load current). Record your results in the table below.

Used a sign wave to see clipping

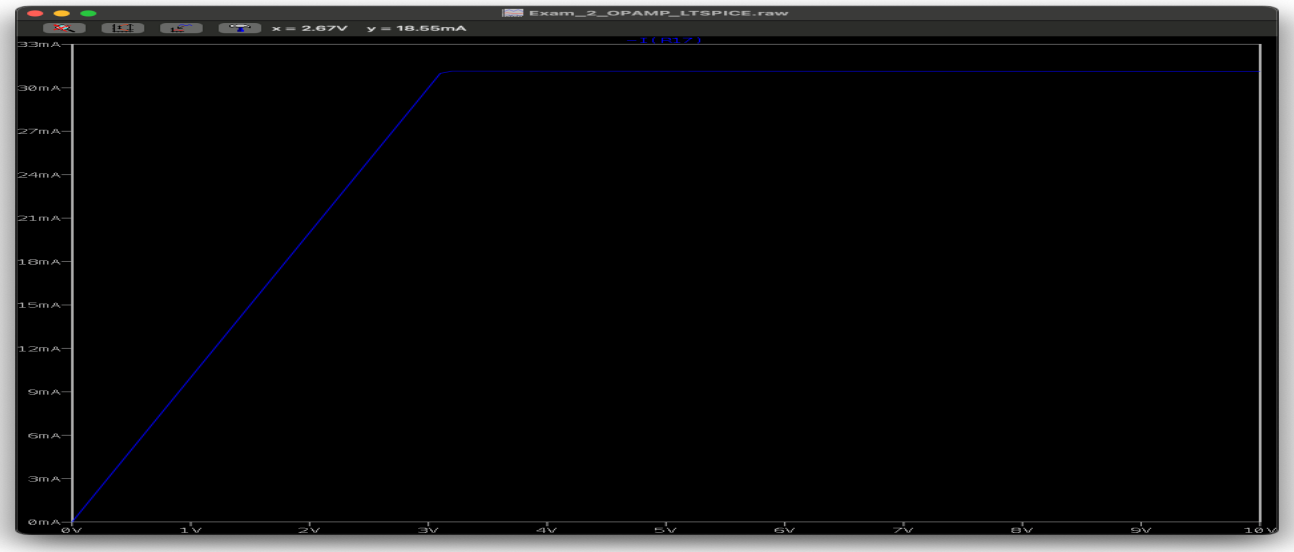
Table 7: Output Swing

Load Resistor (Ohms)	Positive Swing (Volts)	Negative Swing (Volts)	Maximum Load current (mA)
100K	10	-10	.1
10K	10	-10	1
1K	10	-9.85	10
100	4.7	-3.1	48.7

Problem 10: Output Current Limit

Do a hand calculation of the output current limit. Explain your reasoning. Compare to a simulation result. (You will have to put various load resistors on the output in your simulation to test the current limit. At what value does the output begin to current limit? Is the current limit a hard limit (step function) or does the current limit foldback in a continuous fashion? Justify your answer with simulations or analysis.

Analysis on next page. The current is a hard limit, I varied the input voltage with an 100 and 200 ohm resistor on the output and saw that the limit is a hard limit as it saturates at the same current for both values. The limit is 31.82mA.



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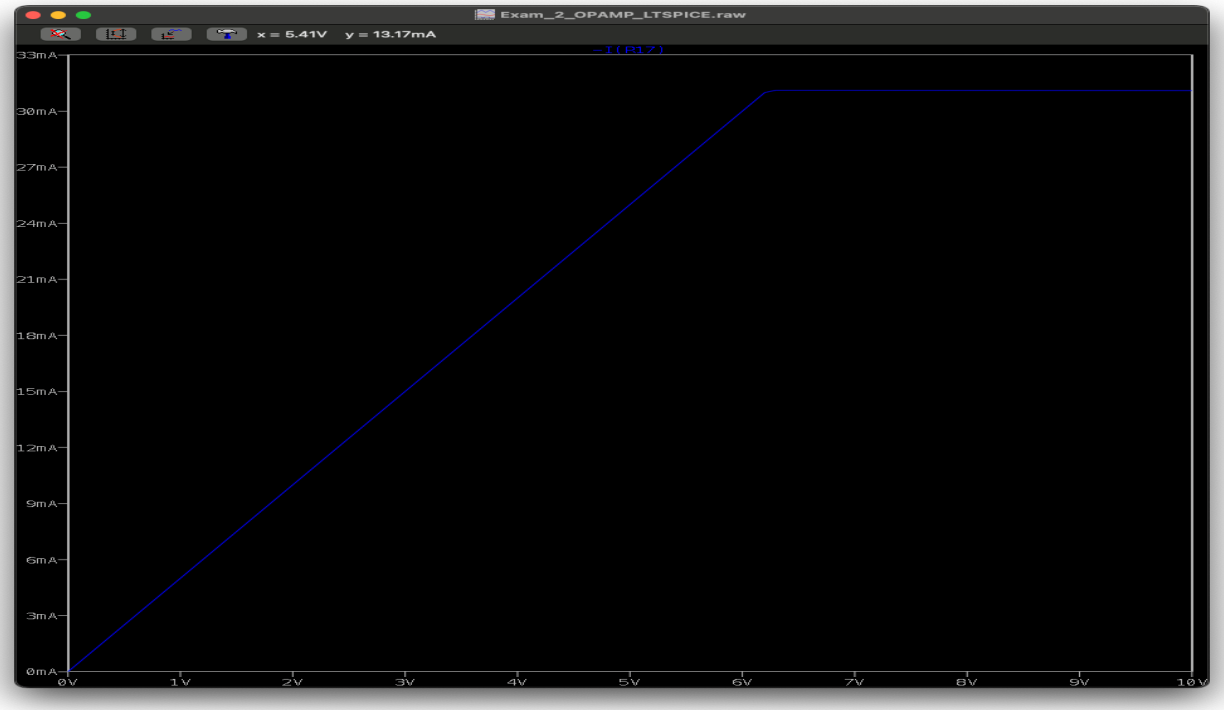
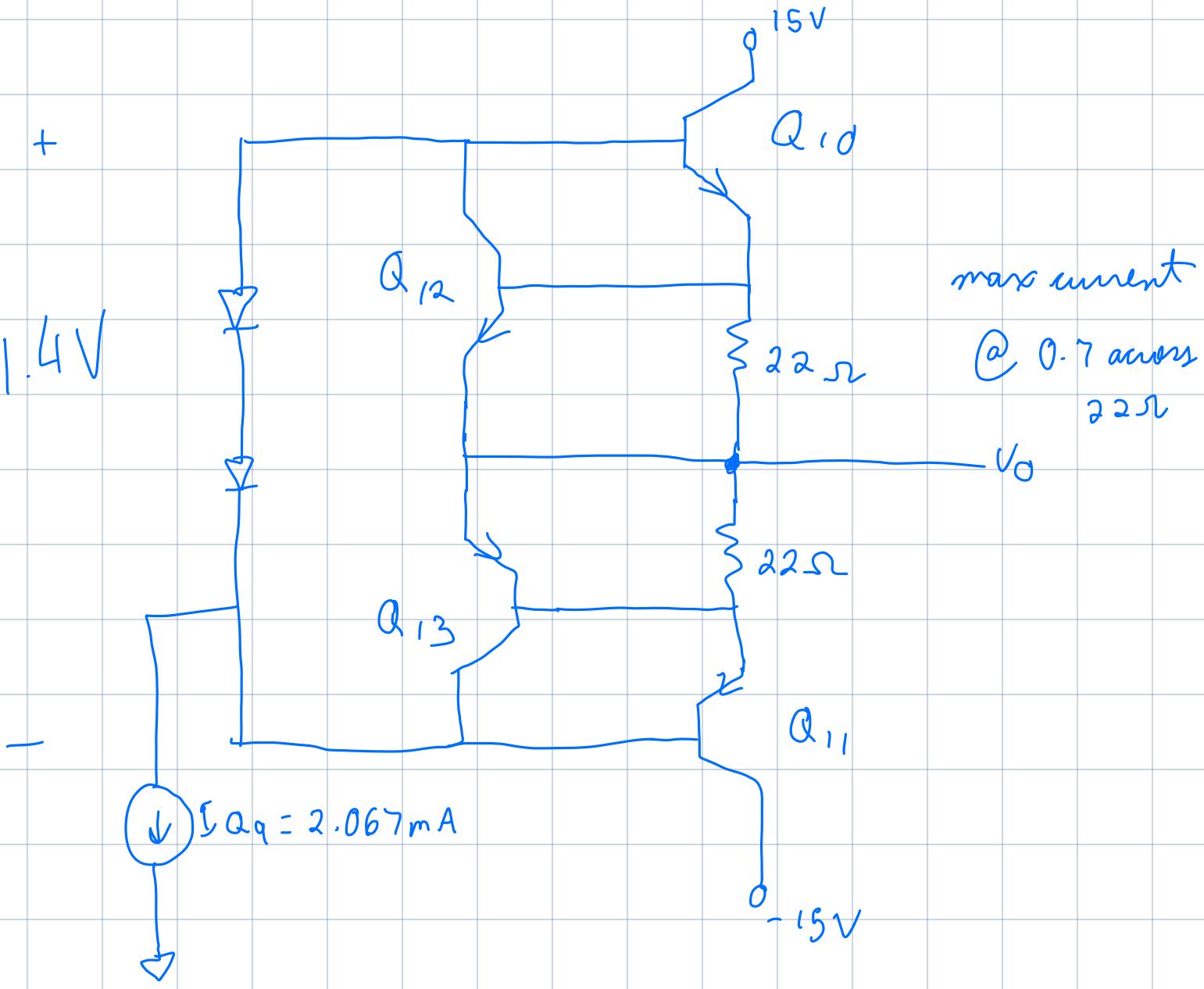


Q_{10}



max current @ 0.7 across 22Ω

$$I_{Q_{10}} = \frac{0.7}{22} = 31.818mA$$

Problem 11: Power Supply Rejection Ratio

Add an AC source in series with the -15V supply. (This should be the only AC supply during this test.) Set the amplitude of the source to 1V. Configure your amplifier for a closed loop gain of 1. Do an AC sweep and look at the AC response of the output. (Your input will be set to 0 for this test. We are only looking at how sensitive the amplifier is to changes on its negative supply.) The ratio of the AC input on the negative supply to the AC output voltage is the Power Supply Rejection Ratio (PSRR). Since we set the AC value to 1 V the output will be the reciprocal of the PSRR. Since you will be plotting in dB you only need to change the sign of the output to get the PSRR. What is the value of the PSRR at low frequencies? Is the PSRR reduced at higher frequencies?

Repeat the analysis with C5 connected between the base of Q3 and ground instead of between the base of Q3 and the negative supply. Does the PSRR change? Which configuration do you believe is better (or are they both the same)? In other words is there a reason to bypass the base to the negative supply instead of ground?

Figures on next page

At low frequencies, the PSRR is high at around 87dB until around 900mHz. At this point there is a valley going down to 63dB at 11Hz and rises back up to 87dB at 1kHz. This then dips linearly to around 0dB at 10MHz. From there is rises and oscillates to 10dB in the GHz region.

The PSRR does not change for most frequencies except for the 1kHz area. When the capacitor is tied to the negative supply the PSRR rises back to 87dB at 1kHz, but when tied to ground, it is only 80dB at 1kHz.

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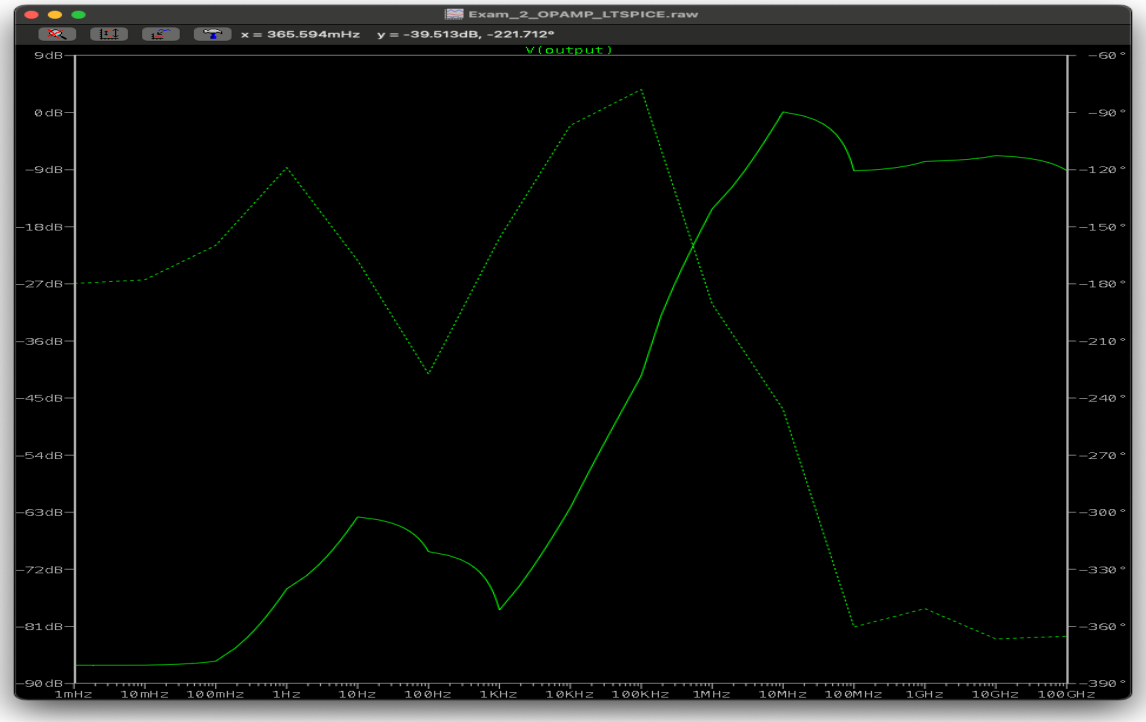
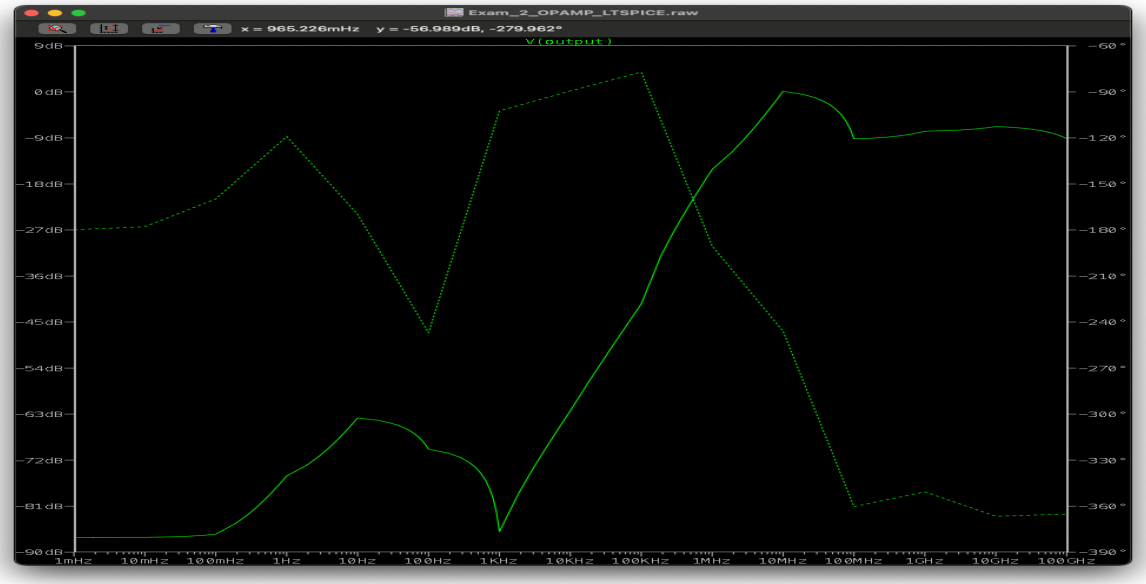


Plot tied to ground



Plot tied to negative supply